debug functions and associated instruction code support into the standard processor. This, of course, increases development cost, chip complexity and chip size. Moreover, such facilities become a part of the processor design which must be carried through and updated as required as enhancements to the original design are developed.

Please replace the paragraph beginning at page 5, line 9 with the following:

An In-Circuit Emulation system breakpoint control consistent with an embodiment of the present invention has a microcontroller and a virtual microcontroller operating in lock-step synchronization. A breakpoint lookup table is associated with the virtual microcontroller with a break bit associated with each of a plurality of instruction addresses, the break bit being set to indicate that a break is to occur at a specified instruction address. A breakpoint controller sends a break message to the microcontroller whenever an instruction address is encountered that is associated with a set break bit.

Please replace the paragraph beginning at page 8, line 21 with the following:

A commercial ICE system utilizing the present invention is available from Cypress MicroSystems, Inc., for the CY8C25xxx/26xxx series of microcontrollers. Detailed information regarding this commercial product is available from Cypress MicroSystems, Inc., 22027 17th Avenue SE, Suite 201, Bothell, WA 98021, in the form of version 1.11 of"PSOC DESIGNER: Integrated Development Environment User Guide", which is hereby incorporated by reference. While the present invention is described in terms of an ICE system for the above exemplary microcontroller device, the invention is equally applicable to other complex circuitry including microprocessors and other circuitry that is suitable for analysis and debugging using in-circuit emulation. Moreover, the invention is not limited to the exact implementation details of the exemplary embodiment used herein for illustrative purposes.

Please replace the paragraph beginning at page 9, line 4 with the following:

Referring now to **FIGURE 2,** an architecture for implementation of an embodiment of an ICE system of the present invention is illustrated as system 200. In system 200, a Host computer 210 (e.g., a personal computer based on a PENTIUM® class microprocessor) is interconnected (e.g., using a standard PC interface 214 such as a parallel printer port connection, a universal serial port (USB) connection, etc.) with a base station 218. The host computer 210 generally operates to run an ICE computer program to control the emulation process and further operates in the capacity of a logic analyzer to permit a user to view information provided from the base station 218 for use in analyzing and debugging a system under test or development.

Please replace the paragraph beginning at page 9, line 29 with the following:

The FPGA of the base station 218 of the current embodiment is designed to emulate the core processor functionality (microprocessor functions, Arithmetic Logic Unit functions and RAM and ROM memory functions) of the Cypress MicroSystems CY8C25xxx/26xxx series microcontrollers. The CY8C25xxx/26xxx series of microcontrollers also incorporates I/O functions and an interrupt controller as well as programmable digital and analog circuitry. This circuitry need not be modeled using the FPGA 220. Instead, the I/O read information, interrupt vectors and other information can be passed to the FPGA 220 from the microcontroller 232 over the interface 226 as will be described later.

Please replace the paragraph beginning at page 10, line 27 with the following:

In the designing of a microcontroller or other complex circuit such as the microcontroller 232, it is common to implement the design using the VERILOG® language (or other suitable language). Thus, it is common that the full functional design description of the microcontroller is fully available in a software format. The base station 218 of the current embodiment is based upon